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Sender: Mary Terry, Patent Secretary for Godfrey K. Kwan

Our Ref. No.: ALTRP116

Your Ref: 10/775,966

Re: Notice of Appeal

Pages Including Cover Sheet(s): 8

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: J. Orion Pritchard et al.

Application No.: 10/775,966

Filed: February 9, 2004

Title: METHODS AND APPARATUS FOR VARIABLE LATENCY SUPPORT

Attorney Docket No.: ALTRP116/A1364

Examiner: Siek, Vuthe

Group: 2825

CERTIFICATE OF FACSIMILE TRANSMISSION:
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office, Commissioner for Patents, Attn: Examiner Siek, Fax No. 571-273-8300, Alexandria, VA 22313-1450 on: January 23, 2007.

Signed: Mary Terry

PRE-APPEAL REQUEST FOR REVIEW

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please consider the following Pre-Appeal Request For Review and remarks provided in response to the Final Office Action dated October 27, 2006.

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

PENDING INDEPENDENT CLAIMS

1. (original) A method for configuring on a programmable chip, the method comprising:

receiving information associated with a primary component, the primary component having either fixed latency or variable latency characteristics;

receiving information associated with a secondary component, the secondary component configurable as either a fixed latency or a variable latency component, wherein the secondary component is operable to respond to requests from the primary component, and

generating an interconnection module coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module supports a system having both fixed latency and variable latency components.

11. (original) A system for configuring a programmable chip, the system comprising:

an input interface configured to receive information associated with a primary component and information associated with a secondary component, the secondary component configurable as either a fixed latency or a variable latency component, wherein the secondary component is operable to respond to requests from the primary component, and

a processor configured to generate interconnection circuitry coupling the primary component to the secondary component, the interconnection module including data, address, and control lines for the programmable chip, wherein the interconnection module supports a system having both fixed and variable latency components

21. (original) A computer readable medium comprising computer code for configuring a programmable chip, the computer readable medium comprising:

computer code for receiving information associated with a primary component, the primary component configurable as either a fixed latency or a variable latency component;

computer code for receiving information associated with a secondary component, the secondary component configurable as either a fixed latency or a variable latency component, wherein the secondary component is operable to respond to requests from the primary component, and

computer code for generating interconnection circuitry coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module support a system having both fixed and variable latency components.

REMARKS

Claims 1-27 are pending. The Examiner rejected claims 1-27 including independent claims 1, 11, and 21 under 35 U.S.C. 120(e) as being anticipated by Oh (6,996,016 B2). The Examiner also rejected claims 1-7, 11-17, and 21-27 under 35 U.S.C. 102(e) as being anticipated by Wingard (6,725,313). Neither Oh nor Wingard teach or suggest all of the elements of the claims.

Oh describes "a system 100 using a burst PSRAM device 104. In one embodiment, the system 100 generally comprises a system controller 102, a memory 104, an address/command (i.e., system) bus 106, and a data (i.e., DQ) bus 108. The memory 104 may comprise one or more component memories (discussed below in reference to FIG. 2), where each component memory is coupled to the buses 106 and 108. The system bus 106 may comprise unidirectional and bi-directional transmission lines, while the DQ bus includes bi-directional transmission lines. The system controller 102 is typically coupled to a processor of an external electronic device 110 (e.g., computer, cell phone, and the like) using an application-specific interface 112.

In one embodiment of the invention, the system bus 106 comprises a bi-directional line 114 (shown in phantom) that transmits a WAIT_DQS signal and a plurality unidirectional transmission lines propagating conventional control and command signals. Such conventional control and command signals comprise, among other such signals, a Clock (CLK) signal, an Address (e.g., 21-bit address word A20-A0) signal, an Address Valid (ADV) signal, a Write Enable (WE) signal, and a Chip Select (CS) signal (all discussed below in reference to FIGS. 3-7)." (column 4, lines 1-24)

Wingard describes a communications systems using multilevel connection identification. "System 1000 includes initiator functional block 1002, which is connected to initiator interface module 1004 by interconnect 1010. Initiator interface module 1004 is connected to target interface module 1006 by shared communications bus 1012. Target interface module 1006 is connected to target functional block 1008 by an interconnect 1010. Typically, shared communications bus 1012 is analogous to shared communications bus 112 of FIG. 1 or to shared communications bus 114 of FIG. 1. Interconnects 1010 are typically analogous to interconnect 115 of FIG. 1 in that they connect functional blocks to interface modules and are point-to-point, rather than shared, interconnects. Interconnects 1010 are typically physically shorter than shared communications bus 1012 because of their local nature. As will be explained more fully below, system 1000 uses two different levels of connection identification depending upon the requirements of a particular functional block. "Global" connection identification information is sent on shared communications bus 1012, while

"local" connection information, or thread identification information, is sent in interconnects 1010." (description of Figure 4)

The Examiner relies on Oh to teach the elements of the claims. It is acknowledged that Figure 1 and the corresponding text do describe a processor 110 and a memory 104 and buses 106 and 108. However, Oh is not believed to teach or suggest receiving information about the primary component and the second component and generating an interconnection module coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module supports a system having both fixed latency and variable latency components.

The Examiner may attempt to argue that receiving this information and generating the interconnection module are inherent in Oh. The Applicants respectfully disagree. The interconnection module in Oh is believed to be a standard bus used to connect components. Primary and secondary components along with buses may be selected and placed without any "receiving information... and generating an interconnection module." Many conventional implementations including Oh, it is believed, use this approach. No interconnection module is generated. In many instances, a standard bus is selected and used as an interconnect. However, the techniques of the present invention recite "receiving information about a primary component and a secondary component" and "generating an interconnection module coupling the primary component to the secondary component." Oh does not teach or suggest any receiving information about a first primary component or receiving any information about a first secondary component. Oh furthermore does not teach or suggest "generating an interconnection module coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module supports a system having both fixed latency and variable latency components."

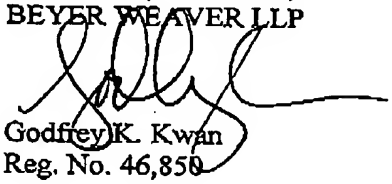
Claim 11 recites an input interface configured to receive information associated with a primary component and information associated with a secondary component ... and a processor configured to generate interconnection circuitry coupling the primary component to the secondary component, the interconnection module including data, address, and control lines for the programmable chip. Oh does not teach or suggest an input interface or any processor configured to perform the above noted elements. Oh only describes a processor connected to a memory over a bus.

The Examiner also relies on Wingard to teach the elements of the claims. Although Wingard shows a master and a slave along with connection lines, Wingard does not teach or suggest "generating interconnection circuitry coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the

interconnection module support a system having both fixed and variable latency components" or "receiving information ... and generating an interconnection module." Again, generating an interconnection module or interconnection circuitry is not inherent. As noted above, primary and secondary components along with buses may be selected and placed without any "receiving information... and generating an interconnection module." Many conventional implementations including Wingard, it is believed, use this approach.

In light of the above remarks relating to the independent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER LLP



Godfrey K. Kwan
Reg. No. 46,850

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100